Report Number: QR-10158.04
Report Period: 22 November 1994
through 22 February 1995

CONTRACT TITLE AND NUMBER:

InP Solar Cell Development on Inexpensive Si Substrates
N00014-94-C-2030

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Contract Period: 22 February 1994 to 22 February 1995

STATUS:

In this report, cell process lots completed in this program to date are summarized below:

***Lots 5752 and 5753 - Feasibility of InGaP or InAlAs Windows for InP Cell on InP***

Purpose: Examine whether InP cell efficiency can be improved by use of a high bandgap pseudomorphic window to reduce surface recombination. PN and NP InP cells on InP wafers were made with 500Å InGaP (1.9 eV) and InAlAs (1.5 eV) windows, as well as no windows (controls). Improvements in the baseline InP cell technology would improve the overall InP/Si cell efficiency.

Result: PN cells with InAlAs windows showed improved photovoltage (860 vs 830 mV) over the control cell, but had lower photocurrent (26 vs. 28 mA/cm$^2$), so that no net gain in efficiency was achieved. Although InAlAs does seem to passivate the P-InP surface (higher $V_{oc}$ despite lower $J_{sc}$ means a much lower dark current), the lattice-matched 1.5 eV InAlAs used absorbs too much light in the window. The PN cell with the InGaP window, and all NP cells showed no significant passivation effects and no net efficiency gains.

Conclusion: Effective InGaP/InAlAs windows are hard to achieve and will not be pursued further in Phase II.

*Lot 5772 - Evaluate the Baseline Efficiency of the Simplest InP/Si Cells Possible*

Purpose: The simplest (thin, least complex) InP/Si cells possible were evaluated to set a baseline to measure future work against. Cells used were PN (no tunnel junction needed) on a thin 2 μm InP buffer (thin epigrowth means less phosphorous cleanup, a manufacturing issue) without any grading layer (no need to control ternary composition or lattice-matching) on a thin-GaAs-coated Si wafer.

Result: Cells were obtained with one sun AM0 efficiencies of 4%, half that obtained in the Phase I program using a PN InP cell on a thick 8 μm InGaP grading layer on a thick GaAs on Si wafer.

Conclusion: The simplest cells are not adequate for this program. Higher efficiency will require more complex epilayers. A useful minimal baseline for InP/Si was achieved. Compared with Phase I work, we infer use of a thick buffer/grade layer on a thick-GaAs-Si wafer doubled the efficiency (8 vs. 4%).

*Lot 5789 - Evaluate the Baseline Efficiency of PN and NP InP Cells on InP*

Purpose: Determine the upper limits of what can be achieved for InP/Si by baselining InP cells on InP. Deliver small (5 mm by 5 mm) InP cells to NRL for radiation experiments.

Result: 19% NP cells made. PN cells epitaxially grown at 650°C better (14%) than 600°C cells (11-12%).

Conclusion: High efficiency NP InP cells easy to make, but need a tunnel junction if made on a Si wafer, since Si is an N-type dopant in InP. PN cells have lower efficiencies, but need no tunnel junction.

*Lot 5796 - Cell Area Scale-Up and Buffer Experiments*

Purpose: Scale PN cells from 1 x 1 cm to 4 x 2 cm. Try thick buffers and InGaP grading layer.

Result: Large 8 $cm^2$ cells were made with efficiencies similar to smaller cells. Efficiencies reached 8%, similar to that achieved in Phase 1. InGaP grade has similar performance to a plain InP buffer layer of similar thickness. This result is again similar to what was seen in Phase I.

Conclusion: Cell scale up does not seem to present any problems on 3-inch Si wafers. Added complexity of a grading layer does not seem justified in terms of performance benefit at this point.

*Lots 5802 - Improve PN InP Cell on InP Wafer Baseline Efficiency*

Purpose: SIMS data of previous PN cells shows that the emitter junction depth, a crucial cell parameter that controls the photocurrent, is not determined by the thickness of the epitaxial emitter layer grown, but is rather controlled by zinc diffusing into the cell from the InGaAs contact cap layer.

Result: Photocurrent of PN InP cells improved from 27 to 30 mA/cm$^2$. Efficiency improved to over 15%.

Conclusion: Emitter junction depth of PN InP cells can be controlled through control of InGaAs cap thickness, which acts as a solid state diffusion source for the zinc P-dopant.

*Lots 5803 - PN vs. NP InP/Si Cell Comparison*

Purpose: NP InP cells have higher baseline efficiency (19%), but when grown on Si wafers require a tunnel junction. PN InP cells had somewhat lower baseline efficiencies (15%), but need no tunnel junction. This experiment seeks to determine which type is most promising. A simple, constant 5μm thick InP buffer was used to lower the dislocations in these cells.

Result: NP InP/Si cells had 11% average efficiency (average $V_{oc}$ 703 mV, $J_{sc}$ 29.6 mA/ cm$^2$, FF 70%) while PN InP/Si cells had 10% efficiency (720 mV, 28.5 mA/cm$^2$, FF 65%).

Conclusion: Fill factor was better for NP than PN, indicating the tunnel junction in the NP design was working well in the NP cell, and that the emitter sheet resistance in the PN design needs to be minimized with a grid redesign. The P-InP emitter in PN cells has about 200x higher sheet resistivity than the N-InP emitter in NP cells. The diffused emitter in the PN cells is 10x deeper (~0.4 μ), so that the sheet resistance is only 20x higher, not 200x. A paper on these cells given at the 1st WCPEC. No clear preference yet for PN or NP.

*Lots 5819 - PN vs NP InP/Si DTG Cells*

Purpose: Grading layers used in previous InP/Si cells were not doing as good a job as expected in reducing the dislocation density. In this experiment, a new proprietary dual temperature growth (DTG) process was implemented to see whether better performance could be achieved. Secondly, we continued to examine both PN and NP cells on Si to see which technology works best. Thirdly, we examined the same NP cell structure grown on a thick-GaAs-coated Si wafer, as opposed to the thin-GaAs-coated wafers we had been previously using in experiments.

Result: NP InP/Si cells had 12% average efficiency (average $V_{oc}$ 738 mV, $J_{sc}$ 29.3 mA/ cm$^2$, FF 73%) while PN InP/Si cells had 9% average (714 mV, $J_{sc}$ 26.5 mA/cm$^2$, FF 63%). For the same NP cell structure using thick vs. thin GaAs-coating on the Si wafer, the

thicker GaAs had on average one third an AM0 percentage point better efficiency (751 mV, 29.2 mA/cm$^2$, FF 74%).

Conclusion: We believe the NP cell technology is a more promising candidate for this program. The tunnel junction seems to present no serious problem. The emitter layer thickness is in the NP cell is determined by the epilayer thickness grown, and is easier to control than in the PN cell, where the emitter thickness/junction depth is controlled by zinc diffusion. Because N-InP has a 20x higher majority carrier higher mobility and can be doped 10x higher than P-InP, the emitters of NP cells have a 200x lower sheet resistivity than PN cells. This allows the emitters to be made thinner, and allows fewer top contact grid metal fingers, both of which allow more photocurrent.

***Lots 5827 - Improved 2cm by 2cm NP InP/Si Cells (NASA cell delivery)***

Purpose: This cell lot was grown as the final deliverable to close out an old NASA InP/Si program that had been inactive at Spire for several years. It is being listed here since it also served as a "free" development run for this current InP/Si cell program, and continued the InP/Si cell development started in this program. In it, we used an optimized version of the best NP cell made in Lot 5819. InGaP and InGaAs grading layers, as well as DTG layers were used to try to reduce dislocations.

Result: Shown in Table 1. Five 2 x 2 cm cells on 3-inch Si wafer make up the average.

**Table 1** *N/P InP/Si cell AM0 25 °C efficiency data.*

| ID Numbers | $V_{OC}$ mV | $J_{SC}$ mA/cm$^2$ | Fill % | η % | Comments |
|---|---|---|---|---|---|
| 3427 average | 751 | 31.4 | 73.2 | 12.6 | 5 μm InP DTG Buffer |
| *3427-2 best cell* | *757* | *31.6* | *73.8* | *12.9* | All 5 cells similar |
| 3428 average | 754 | 31.5 | 72.4 | 12.5 | 5 μm InP DTG Buffer |
| ***3428-2 best cell*** | ***761*** | ***31.8*** | ***74.3*** | ***13.1*** | All 5 cells similar |
| 3429 average | 481 | 27.5 | 59.4 | 5.7 | 7 μm InGaAs Grade Expt |
| *3429-3 best cell* | *486* | *27.6* | *61.0* | *6.0* | All 5 cells similar |
| 3430 average | 754 | 31.0 | 64.2 | 10.9 | 5 μm InP DTG Buffer |
| *3430-2 best cell* | *760* | *30.8* | *73.6* | *12.6* | 1 very bad cell out of 5 |
| 3431 average | 719 | 29.2 | 65.5 | 10.0 | 7 μm InGaP Grade Expt |
| *3431-5 best cell* | *732* | *29.0* | *69.4* | *10.7* | 1 cell out of 5 lower eff. |

Conclusion: Grading layers are still ineffective. DTG buffers are simpler and work better. Best cell is 13.1%. When the NASA program became inactive several years ago, the best NP InP/Si cell was 9.9%. The improvement of 30% in efficiency is the result of this Navy program. In addition, the current cells are much more uniform and reproducible than in the past NASA program.

*Lots 5832 - Optimize InP Growth Temperature, Emitter Thickness, Explore MQW Cells*

Purpose: When we were evaluating PN InP cells, we were surprised at how much better cells grown at 650°C were than cells grown at 600°C, our normal temperature (see Lot 5789). We went to 650°C to control the zinc diffusion in the PN cells. In NP cells, this was not an issue, and all past Spire NP cells, were grown at 600°C. We wished to see if 650°C growth would also improve the NP cell. Secondly, we also wanted to try to make the emitter thinner, to increase the amount of photocurrent generated in the base layer, where it is protected from surface recombination. Finally, Dr. Neal Anderson of Univ. of Massachusetts, Amherst designed some InP multiquantum well cells which might improve the photocurrent, and those cells were grown and piggypacked onto this process lot.

Result:
a) 600°C ($V_{oc}$ 880 mV, $J_{sc}$ 34 mA, FF 85%) vs. 650°C (880 mV, 33 mA, 81%)
b) ~400Å emitter (880 mV, 34 mA, 85%) vs. ~200Å emitter (873 mV, 35 mA, 84%)
c) Multiquantum well cells had some extra photocurrent response at wavelengths above the 920 nm InP cutoff wavelength, but had poor photovoltage and lower quantum efficiency below 920 nm.

Conclusion: 600°C and 650°C cells similar, but 600°C slightly better. Using a thin emitter increased photocurrent slightly, but also decreased photovoltage (more dark current) and fill factor (more resistance), for no net gain, so we will continue to use thicker emitter. MQW cells are a long term project.

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